

The VFAT3-Comm-Port: a complete communication port for front-end ASICs intended for use within the high luminosity radiation environments of the LHC

This content has been downloaded from IOPscience. Please scroll down to see the full text.

2015 JINST 10 C03019

(<http://iopscience.iop.org/1748-0221/10/03/C03019>)

View [the table of contents for this issue](#), or go to the [journal homepage](#) for more

Download details:

IP Address: 134.58.253.57

This content was downloaded on 17/03/2015 at 12:55

Please note that [terms and conditions apply](#).

RECEIVED: November 4, 2014

REVISED: December 17, 2014

ACCEPTED: January 7, 2015

PUBLISHED: March 16, 2015

TOPICAL WORKSHOP ON ELECTRONICS FOR PARTICLE PHYSICS 2014,
22–26 SEPTEMBER 2014,
AIX EN PROVENCE, FRANCE

The VFAT3-Comm-Port: a complete communication port for front-end ASICs intended for use within the high luminosity radiation environments of the LHC

M. Dabrowski,^{a,b,1} P. Aspell,^a S. Bonacini,^a D. Ciaglia,^a G. De Lentdecker,^c
G. De Robertis,^d K. Kloukinas,^a M. Kupiainen,^e P. Leroux,^b F. Tavernier,^b J. Talvitie^e
and T. Tuuva^e

^aCERN – European Center for Nuclear Research,
1211 Geneva 23, Switzerland

^bKatholieke Universiteit Leuven,
Oude Markt 13, 3000 Leuven, Belgium

^cUniversite Libre de Bruxelles,
AV. F. Roosevelt 50, 1050 Brussels, Belgium

^dIstituto Nazionale di Fisica Nucleare – Sezione di Bari,
Via E. Orabona n. 4, 70125 Bari, Italy

^eLappeenranta University of Technology,
Skinnarilankatu 34, 53850 Lappeenranta, Finland

E-mail: mieczyslaw.dabrowski@cern.ch

ABSTRACT: This paper presents the VFAT3 Comm-Port (V3CP), which offers a single port for all communication to and from a front-end ASIC within the HL-LHC environment. This includes synchronization to the LHC clock, slow control communication, the execution of fast control commands and the readout of data.

KEYWORDS: Radiation-hard electronics; Front-end electronics for detector readout; Digital electronic circuits

¹Corresponding author.

Contents

1	Introduction	1
2	General architecture	2
2.1	Basic principle	2
3	V3CP functions	3
3.1	Reception of 320 Mbps serial data and synchronization to the 40 MHz LHC clock	3
3.2	Encoding/decoding of input data	4
3.2.1	VFAT3 downlink codes	4
3.3	Communication with the Slow Control	4
3.4	Transmission of data from V3CP to GBTX	6
4	Conclusion	7

1 Introduction

CMS is currently planning extensive detector and electronics upgrades to take full advantage of the high luminosity environment of the HL-LHC. As part of this upgrade, GEM detectors are planned to be added to the forward regions of the CMS Muon system where the particle rate is at its peak. Together with new electronics, the GEM system will provide improved trigger efficiency and improved precision of tracking in the high eta region.

Key “on-detector” components of the electronics system are the front-end readout ASIC and the GigaBit Transceiver (GBTX) [1], as shown in figure 1. The front-end ASIC is based on the VFAT series [2] of which the VFAT2 chip has already been widely used for the readout of GEM detectors in TOTEM during the first phase of the LHC. The HL-LHC requirements however necessitate a new front-end ASIC which is known as VFAT3. The GBTX is a chip set for optical reception and transmission of all data in and out of the system and has been developed as a common project for use in many HL-LHC detector systems.

A key design specification for the VFAT3 ASIC is direct compatibility with the GBTX which communicates with front-end chips via e-links [3–5]. The V3CP is the communication port within VFAT3 that connects directly to the GBTX.

The main design goal for the V3CP was to have a block through which all chip communication passes through a single port. This includes fast control commands, readout data and bi-directional slow control communication.

The key benefits of the V3CP port are the following:

- Only one port is needed on the front-end ASIC.

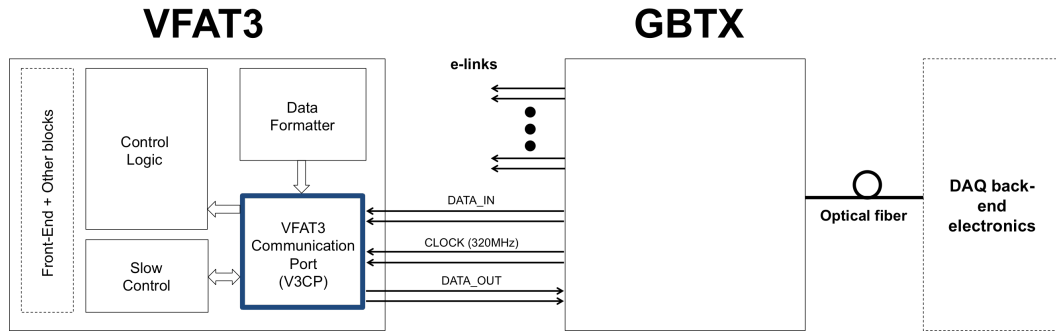


Figure 1. The connection between the VFAT3 chip and the GBTX chip in the CMS GEM Data-acquisition system [6].

- Removes the need for an additional slow control interface such as I²C. This in itself removes the need for an addition slow control path on the board and its interface chip, simplifying the system design.
- Much faster Slow-Control communication, which is useful for system set-up and calibration processes.

2 General architecture

2.1 Basic principle

The V3CP is designed to operate with the e-links running at 320 Mbps. 320 Mbps allows the use of 8 bit serial codes to be delivered to chip, each code representing a particular command per LHC bunch crossing. Figure 2 shows the codes as arbitrary command functions EC0, BC0.. (full list of control commands can be found in section 3.2.1). These codes are decoded to individual command signals synchronous to the LHC machine clock to be acted upon within the chip. For this to happen, frame synchronization of the link must first be achieved. This is done by the detection of comma characters in code sequence which are phase insensitive — they cannot appear in any combination of normal codes. At the same time an internal 40 MHz sampling clock is derived from the 320 MHz clock delivered by the GBTX. It is phase aligned to the LHC clock via the comma character detection. Once synchronization is achieved all the other codes can be detected. Communication with the slow control is done by using two codes, one which represents a logic “zero” to be sent to the slow control block and one which represents a logic “one” (SC0 and SC1).

The functions of the V3CP can therefore be summarized as:

- Reception of 320 Mbps serial data and synchronization to the 40 MHz LHC clock.
- Detection and decoding of synchronous control commands.
- Separation and prioritized interleaving of data types, detector data and slow control data.
- Transmission of data to the GBTX.

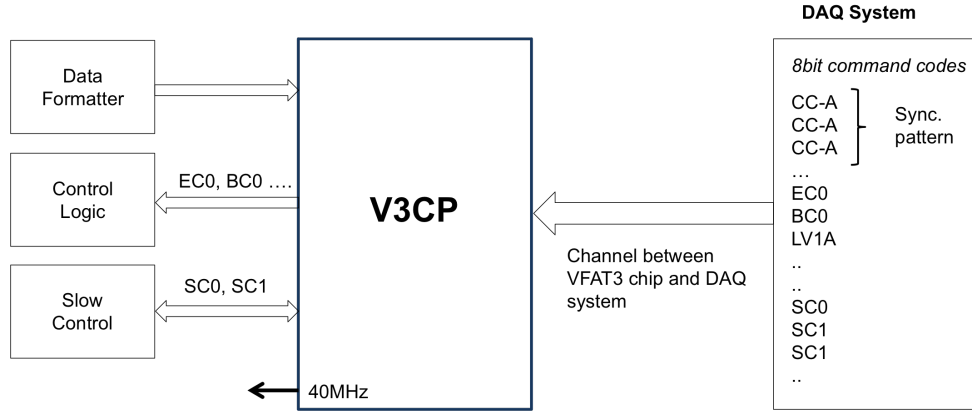


Figure 2. Communication with the V3CP from a user's perspective.

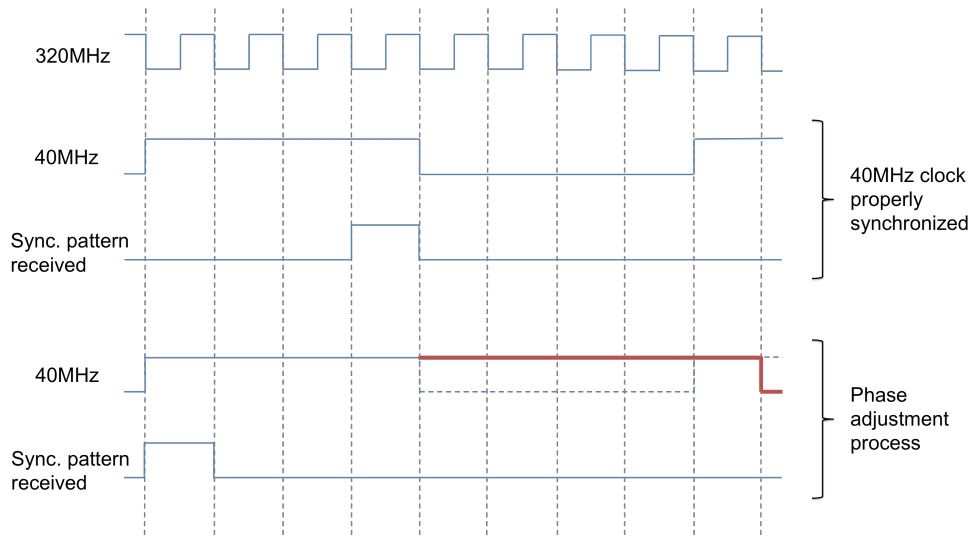


Figure 3. 1) Relation between the phase of the 40 MHz clock and the moment of the reception of the synchronization pattern. 2) The process of the phase adjustment of 40 MHz clock.

3 V3CP functions

3.1 Reception of 320 Mbps serial data and synchronization to the 40 MHz LHC clock

The incoming 320 Mbps serial data stream is shifted into a shift register and de-multiplexed into 8 bit words. In addition, a 40 MHz internal clock is derived through division of the 320 MHz clock received on the “Clock” input.

Phase alignment to the 40 MHz machine clock is achieved by detection of a 24-bit synchronization pattern which is composed of three consecutive comma characters (CC-A — table 1). After detection of the synchronization pattern, the phase adjustment of the 40 MHz clock starts. The 40 MHz clock is stopped and held for the period of one up to seven clock cycles of the 320 MHz clock. Such a phase synchronization technique makes sure that no glitches would occur in the blocks driven by that clock. The timing relationship for this process is shown in figure 3.

The synchronization process also provides frame alignment of the incoming data stream such that phase aligned 8 bit words are latched correctly into the 40 MHz domain.

Verification that the internal 40 MHz clock is properly phase aligned is possible via a separate comma character (CC-B). Once the CC-B pattern is recognized, the V3CP checks the phase of the 40 MHz clock. If the clock is synchronized properly V3CP signals that by transmitting the synchronization acknowledge header to the DAQ system.

3.2 Encoding/decoding of input data

Typical of most front-end systems is an asymmetry in the bandwidth requirements for the data paths to and from the front-end ASIC. Relatively few commands are required to be transmitted to the front-end ASIC (downlink) whilst maximum bandwidth must be obtained in the uplink. Since the GBTX operates with equal bandwidths for both down and up link data, there is a redundancy on the downlink path.

This downlink redundancy can be put to good use by encoding the commands sent to the front-end. The GBTX provides the fixed-latency path. This permits 8 bits to be transmitted per bunch crossing when using the 320 MHz e-link.

The uplink however does not require encoding and the full bandwidth can be exploited.

Two different encoding schemes were considered for the V3CP downlink, namely: 7-to-8 bit encoding [7] and 4-to-8bit encoding [8].

The 7-to-8 bit encoding scheme provides one comma character, 128 possible data words and DC balancing.

The 4-to-8 bit encoding provides two comma characters, 16 data words, DC balancing possible and in addition it provides Single-Error-Correction (SEC) and Double-Error-Detection (DED) capabilities.

The number of commands required in the downlink to VFAT3 is less than 16. Therefore, the 4-to-8 bit encoding could be used with the advantage of providing SEC and DED when operating with a 320 MHz e-links as currently foreseen for the GEM system. This encoding scheme hence increases the robustness to input data errors that can appear on the transmission lines and also increases robustness to Single Event Effects (SEEs) after data are latched and processed inside a chip.

Please note, that only the decoding process is implemented in the V3CP. The encoding should be performed in the device which transmits data to the chip. It can be implemented in software, firmware or hardware.

3.2.1 VFAT3 downlink codes

The complete set of downlink codes (FSCCs) is listed in table 2. Idle characters could be A and P which should be sent alternately.

3.3 Communication with the Slow Control

The Data Controller handles communication with the Slow Control, the Control Logic and the Data Formatter of the VFAT3 chip. The architecture of V3CP is presented in figure 4.

The user communicates with the Slow Control via the HDLC protocol [9] which sits at a higher level to the encoding/decoding of Fast Synchronous Control Commands. Each “logic 0”

Table 1. Transmission codes provided by 4-to-8 bit coder.

Name	4-bit word	8-bit representations	Disparity
A	0000	00000000	−4
B	0001	00001111	0
C	0010	00110011	0
D	0011	00111100	0
E	0100	01010101	0
F	0101	01011010	0
G	0110	01100110	0
H	0111	01101001	0
I	1000	10010110	0
J	1001	10011001	0
K	1010	10100101	0
L	1011	10101010	0
M	1100	11000011	0
N	1101	11001100	0
O	1110	11110000	0
P	1111	11111111	+4
CC-A		00010111	0
CC-B		11101000	0

Table 2. List of the Fast Synchronous Control Commands (FSCCs).

FSCC	Character	Function
EC0	B	Reset of the Event Counter (EC)
BC0	C	Reset of the BCZ Counter (BC)
CalPulse	D	Injection of the Calibration Pulse
ReSync	E	Resets all VFAT3 state machines
SCOnly	F	Force „Slow Control Only” Mode
RunMode	G	Return from „Slow Control Only” Mode
LV1A	H	First Level Trigger
SC0	I	Sends „0” to the Slow Control
SC1	J	Sends „1” to the Slow Control
ReSC	K	Reset of Slow Control
LV1A+EC0	L	First Level Trigger and reset of the EC
LV1A+BC0	M	First Level Trigger and reset of the BC
LV1A+EC0+BC0	N	First Level Trigger and reset of the EC and the BC
EC0+BC0	O	Reset of the EC and the BC

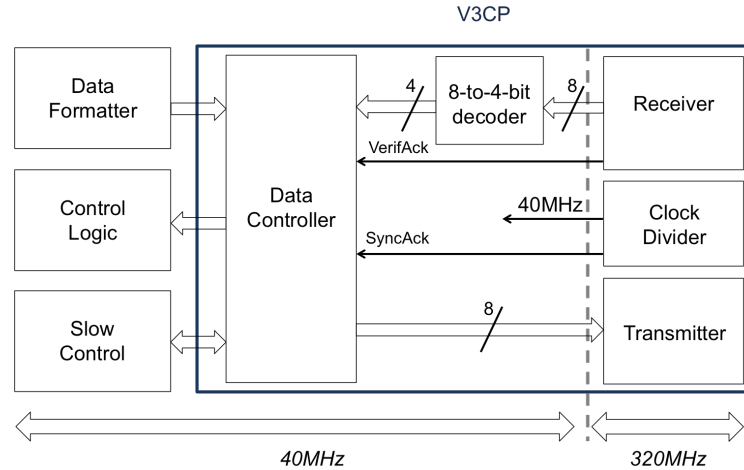


Figure 4. The architecture of V3CP.

and “logic 1” of the HDLC protocol is encoded to SC0 and SC1 8 bit codes before transmission to VFAT3. After decoding within the V3CP, the Data Controller routes the SC0 and SC1 bits to the Slow Control unit.

The same is true for the Slow control response in that each bit from the Slow Control unit is encoded to 8 bit SC0 and SC1 codes before transmission from VFAT3. This allows the user to have an effective bandwidth of 40 MHz communication with the Slow Control unit which is significantly faster than the commonly used slow communication protocol of I²C.

The VFAT3 Slow Control system allows the Data Controller to perform seamless prioritized interleaving between the different types of data. This is because the HDLC data stream can be interrupted and resumed without any consequence.

There are two different modes of operation controlling the prioritizing of data types; “Run Mode” and “Slow Control Only” (SCOnly) mode. In “Run Mode”, tracking data from the Data Formatter has the priority over the data coming from the Slow Control unit. Operation in “Run Mode” is aimed at normal operation. The SCSOnly mode, as the name suggests, forces communication to and from the Slow Control unit ignoring data from the Data Formatter. This is the default mode after power-on of the chip.

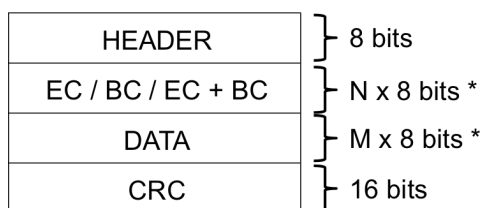
3.4 Transmission of data from V3CP to GBTX

There are two types of data transmitted. These are tracking data, which comprise information on detector channels hit, and Slow Control data. The transmission of data from VFAT3 is through a serial bit stream of 320 Mbps. This bit stream is frame aligned through the use of 8 bit headers. Table 3 shows the list of headers transmitted from VFAT3.

Following the initial chip synchronization procedure a SyncAck header is sent. Frame alignment in the DAQ system can be achieved either by detecting this header or aligning to the filler headers F1 and F2 which are continually transmitted from the chip alternately when there is no other information to transmit.

Table 3. List of headers that are transmitted from the chip to the outside world.

FSCC	8-bit representation	Function
SC0	10010110	Slow Control „0”
SC1	10011001	Slow Control „1”
F1	11111110	Filler 1
F2	11111101	Filler 2
SyncAck	10101111	Synchronization acknowledge
VerifAck	11111010	Verification acknowledge

**Figure 5.** Data packet which comprises a header, a time tag, tracking data and a CRC check code. * N and M depend on the chip’s internal settings.

Headers are also used for the transmission of SC0 and SC1 bits as explained in the previous section.

During “Run Mode” the tracking data has priority. Following “LV1A” triggers, VFAT3 constructs data packets for each trigger within the Data Formatter. The data packets (an illustration of data packet can be found in figure 5) are self contained consisting of a header, tracking data, time tag information and a CRC check code. These data packets are programmable in content and not further explained here. They are transmitted without encoding to allow use of the full bandwidth of the link.

4 Conclusion

The VFAT3-Comm-Port (V3CP) is a complete communication port, designed to provide bi-directional communication of all data types to and from front-end ASICs, particularly VFAT3. It is designed for operation in demanding radiation environments and to be compatible with the GigaBit Transceiver (GBTX) chip. The port provides a communication protocol which enables synchronization of a chip within a large system and adds robustness against SEEs and SEUs that can occur during transmission. Its specific implementation within VFAT3 allows communication with the Slow Control with an effective bandwidth of 40 Mbps, which can decrease the time that is needed for the chip characterization, system setup and system calibration. For robustness against SEUs and SEEs, the V3CP logic was designed using Triple Module Redundancy.

References

- [1] K. Wyllie et al., *A Gigabit Transceiver for Data Transmission in the Future High Energy Physics Experiments*, *Phys. Procedia* **37** (2012) 1561.
- [2] P. Aspell et al., *VFAT2: A front-end “system on chip” providing fast trigger information, digitized data storage and formatting for the charge sensitive readout of multi-channel silicon and gas particle detectors*, *IEEE Nucl. Sci. Symp. Conf. Rec.* **2008** (2008) 1489.
- [3] S. Bonacini et al., *E-link: A Radiation-Hard Low-Power Electrical Link for Chip-to-Chip Communication*, presented at *Topical Workshop on Electronics for Particle Physics*, Paris, France, 21–25 September 2009, pg. 422.
- [4] F. Tavernier et al., *A radiation-hard PLL for frequency multiplication with programmable input clock and phase-selectable output signals in 130 nm CMOS*, *2012 JINST* **7** C12014.
- [5] F. Tavernier et al., *The eCDR, a Radiation-Hard 40/80/160/320 Mbit/s CDR with internal VCO frequency calibration and 195 ps programmable phase resolution in 130 nm CMOS*, *2013 JINST* **8** C12024.
- [6] G. De Lentdecker et al., *Development of the data acquisition system for the Triple-GEM detectors for the upgrade of the CMS forward muon spectrometer*, *2014 JINST* **9** C03052.
- [7] S. Bonacini, *7-to-8bit encoding scheme*, CERN Internal document (2012).
- [8] M. Dabrowski, *4-to-8bit encoding scheme, which provides Single-Error Correction and Double-Error detection capabilities*, CERN Internal document (2013).
- [9] *Telecommunications and information exchange between systems – High-level data link control procedures*, ISO/IEC 13239 (2002).